Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-2. (Cancelled).

3. (Currently amended) A computer system, comprising:

a plurality of processors coupled together between which messages can be routed;

an I/O controller coupled to one or more of said processors;

at least one I/O device coupled to an I/O controller; and

wherein each processor is capable of detecting an error in a message sent from another processor in the system and reformatting the message to indicate to other of said processors that the message contains a transmission error; ~~The computer system of claim 1~~

wherein each of said messages between said processors comprises a header ticks and data tick~~multiple ticks~~, ~~each~~ the data tick comprising ~~multiple bits of information including~~ error check bits, and wherein upon detecting an error has occurred in ~~a tick~~the message, the processor alters the data tick error check bits in a predetermined manner to indicate to other of said processors that the message contains an error.

4. (Currently amended) A computer system, comprising:

a plurality of processors coupled together between which messages can be routed;

an I/O controller coupled to one or more of said processors;

at least one I/O device coupled to an I/O controller;

wherein each processor is capable of detecting an error in a message sent from another processor in the system and reformatting the message to indicate to other of said processors that the message contains a transmission error; ~~The computer system of claim wherein 1~~

wherein each of said messages between said processors comprises a header tick and a data tick~~multiple ticks~~, each tick comprising multiple bits of information, and wherein upon detecting an error has occurred in a data tick, the processor replaces the bits of information in the data tick with a predetermined bit pattern.

5. (Original) The computer system of claim 4 wherein said predetermined bit pattern includes a known double bit error code.

6.-9. (Canceled).

10. (Currently amended) A processor, comprising:

a memory controller that coordinates transactions to a memory device; and

a router coupled to said memory controller and providing interfaces to one or more other processors;

wherein said router is capable of detecting a transmission error in a message received from another processor and reformatting the message to indicate that the message contains a transmission error that has already been detected; ~~The processor of claim 8~~

wherein said message comprises ~~multiple sequential~~a data block ~~s of data~~ and a block comprising ~~, each data block comprising multiple bits of information including~~ error check bits, and wherein upon detecting that a transmission error has occurred in ~~a data block~~ the message, the router alters the ~~data block~~ error check bits in a predetermined manner to indicate that the message contains a transmission error.

11. (Currently amended) A processor, comprising:

a memory controller that coordinates transactions to a memory device; and

a router coupled to said memory controller and providing interfaces to one or more other processors;

wherein said router is capable of detecting a transmission error in a message received from another processor and reformatting the message to

indicate that the message contains a transmission error that has already been detected; ~~The computer system of claim wherein 8~~

wherein said message comprises ~~multiple sequential~~ a data block ~~s of data~~ and a header block, ~~each data block comprising multiple bits of information,~~ and wherein upon detecting that a transmission error has occurred in ~~a~~ the data block, the router replaces the bits of information in the data block with a predetermined bit pattern.

12. (Original) The computer system of claim 11 wherein said predetermined bit pattern includes a known double bit error code.

13.-14. (Canceled).

15. (Original) A method of fault isolation in a multi-processor computer system, comprising:

(a) receiving a message;

(b) detecting an error in said message;

(c) replacing the erroneous portion of said message with a predetermined bit pattern to indicate to other processors in said system that an error has occurred in said message and said error has already been detected; and

(d) transmitting the message to another processor in said system.

16. (Canceled).

17. (Original) The method of claim 15 further including:

(e) alerting the system that a fault has been detected in said message.

18. (Currently amended) The method of claim 17 further including:

(f) receiving said message that has been altered in (c);

(g) determining whether said message includes said predetermined bit pattern; and

(h) if said message includes said predetermineds bit pattern, not alerting the system that a fault is present in said message.

19. (Original) The method of claim 18 further including:

(i) transmitting said message with said predetermined bit pattern to another processor in said system.

20. (Currently amended) The method of claim 15 further including:

(j) receiving said message that has been altered in (c);

(k) determining whether said message includes said predetermined bit pattern; and

(l) if said message includes said predetermined[[s]] bit pattern, not alerting the system that a fault is present in said message.

21. (Original) The method of claim 20 further including:

(m) transmitting said message with said predetermined bit pattern to another processor in said system.